正基科技股份有限公司

SPECIFICATION

PRODUCT NAME：AP6781P

REVISION：0.6

DATE：Dec. 1st , 2023

Customer APPROVED	
Company	
Representative Signature	

PREPARED	REVIEW			APPROVED	DCC ISSUE
	PM	QA	ET		

正基科技股份有限公司

AMPAK Technology Inc.

AP6781P

Data Sheet

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Revision

Revision	Date	Description	Revised By
0.1	2023/3/1	-- Preliminary release	Ares
0.2	2023/4/13	-- Updated RF performance	Ares
0.3	2023/4/18	--Add 802.15.4 Thread	Ares
0.4	2023/5/02	--Updated Dimension	Ares
0.5	2023/05/05	-- Modify 6e RF channels	Ares
0.6	2023/12/01	-- Modify Wi-Fi RF Specification	Darren

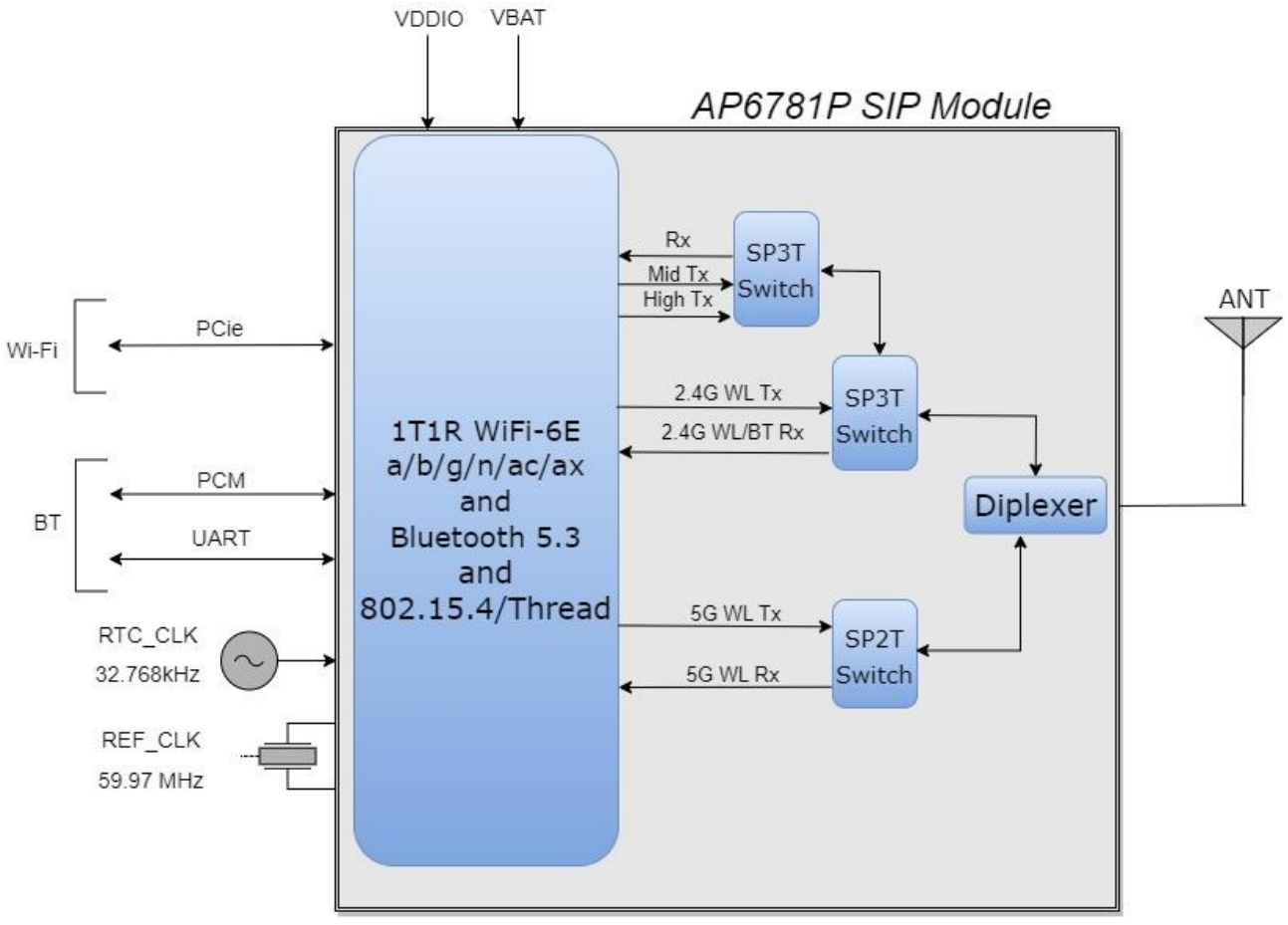
Contents

1. Introduction

1.1 Overview

The AMPAK Technology® AP6781P is a fully Wi-Fi and Bluetooth and IEEE 802.15.4/Thread functionalities module with seamless roaming capabilities and advance security, also it could interact with different vendors' Wi-Fi 6E or legacy Access Points / Routers and run up to PHY rate of 600Mbps with single stream. Furthermore, AP6781P included PCIe interface for Wi-Fi, UART/ PCM interface for Bluetooth and UART interface for IEEE 802.15.4/Thread.

In addition, this compact module is a total solution for a combination of Wi-Fi + BT technologies. The module is specifically developed for tablet, OTT box and portable devices.



1.2 Product Features

IEEE 802.11 Key Features

- 802.11ax/ac/a/b/g/n compliant
- Radio band support for 2.4 / 5 / 6 GHz band including 6GHz UNII-5,6,7,8
- Support 802.11ax & legacy for 2.4 / 5 GHz band
- Support 802.11ax only for 6GHz band
- Lead-free & Halogen-free design which is compliant with ROHS requirements.
- TX and RX low-density parity check (LDPC) support for improved range and power efficiency.
- Single-stream spatial multiplexing up to 600 Mbps data rate.
- 20, 40, 80 MHz bandwidth channels with optional SGI (1024 QAM modulation) for 5 / 6 GHz bands
- 20MHz channels for 2.4 GHz band with optional SGI (1024 QAM modulation)
- Supports PCI express revision 3.0 and power management running at Gen1 speeds.

Bluetooth Key Feature

- BT host digital interface:
  - HCI UART (up to 4 Mbps)
  - PCM for audio data
- Complies with Bluetooth Core Specification Version 5.3 with provisions for supporting future specifications. With Bluetooth Class 1 or Class2 transmitter operation.
- Supports extended synchronous connections (eSCO), for enhanced voice quality by allowing for retransmission of dropped packets.
- Adaptive frequency hopping (AFH) for reducing radio frequency interference.
  A simplified block diagram of the module is depicted in the figure above.
- BT Core Specification Version 5.3, including the following support:
  - Low energy(LE) isochronous channels
  - LE power control
  - LE enhanced connection update
  - LE channel classification
  - LE audio

IEEE 802.15.4/Thread Key Feature

- Support IEEE 802.15.4/Thread that can act as Border Router.

2. General Specification

2.1 General Specification

Model Name	AP6781P
Product Description	1T1R 802.11 a/b/g/n/ac/ax Wi-Fi 6E + BT 5.3+ IEEE 802.15.4/Thread
Dimension	L x W : 12 x 12 (typical) mm，H : 1.95 (Maximum) mm
WiFi Interface	Support PCIe v3.0 compliant and runs at Gen2 speeds.
BT Interface	UART / PCM
Operating temperature	-40°C to 85°C
Storage temperature	-40°C to 125°C
Humidity	Operating Humidity 10% to 95% Non-Condensing

Note: The optimal RF performance specified in the data sheet, however, is guaranteed only -10 °C to +55 °C and 3.2V < VBAT < 3.8V without derating performance.

2.2 DC Characteristics

2.2.1 Absolute Maximum Ratings

Symbol	Description	Min.	Max.	Unit
VBAT	Input supply Voltage	3.0	5.25	V
VDDIO	Digital/Bluetooth/SDIO/ I/O Voltage	1.62	1.95	V

Note : RF performance is optimal for 3.2V ≤ VBAT ≤ 5.0V. For 2.5 V≤VBAT ≤3.2V, device radios will operate but RF performance will degrade.

2.2.2 Recommended Operating Rating

The module requires two power supplies: VBAT and VDDIO.

Voltage rails	Min.	Typ.	Max.	Unit
VBAT	3.2	3.3	3.8	V
VDDIO	1.62	1.8	1.98	V

VBAT current consumption 1000mA(Peak), when VBAT = 3.3V

The module requires two power supplies: other Digital I/O Pins.

For VDDIO=1.8V	Min.	Max.	Unit
Input high voltage	0.65 x VDDIO	NA	V
Input low voltage	NA	0.35 x VDDIO	V
Output high voltage @ 2mA	VDDIO – 0.4	NA	V
Output low voltage @ 2mA	NA	0.4	V

3. Wi-Fi RF Specification

3.1 2.4GHz RF Specification

Conditions : VBAT=3.3V ; VDDIO=1.8V ; Temp:25°C

Feature	Description
WLAN Standard	IEEE 802.11 b/g/n/ax & Wi-Fi compliant
Frequency Range	2400 MHz ~ 2483.5 MHz (2.4GHz ISM Band)
Number of Channels	2.4GHz：Ch1 ~ Ch13
Modulation	802.11b : DQPSK、DBPSK、CCK 802.11g/n : OFDM /64-QAM、16-QAM、QPSK、BPSK 802.11ax : OFDMA /256-QAM、64-QAM、16-QAM、QPSK、BPSK

Output Power , tolerance ± 1.5 dB

The transmit EVM quality & spectrum mask are compliant with IEEE 802.11 standard

802.11b	1Mbps	2Mbps	5.5Mbps	11Mbps	
	19	19	19	19	
802.11g	6、9Mbps	12、18Mbps	24Mbps	36Mbps	48Mbps
	19	19	19	18	18
	54Mbps				
	18				
802.11n 20MHz	MCS0~2	MCS3	MCS4	MCS5	MCS6
	19	19	18	18	18
	MCS7				
	18				
802.11ax 20MHz	HE0~2	HE3	HE4	HE5	HE6
	19	19	18	18	18
	HE7	HE8	HE9	HE10	HE11
	18	18	18	17.5	17.5

	Dara rate	Tones	Spec.(dBm)	Dara rate	Tones	Spec.(dBm)
802.11ax_20MHz SISO_OFDMA	HE0	26	19	HE6	26	18
		52	19		52	18
		106	19		106	18
		242	19		242	18
	HE1~2	26	19	HE7	26	18
		52	19		52	18
		106	19		106	18

		242	19		242	18
	HE3	26	19	HE8	26	18
		52	19		52	18
		106	19		106	18
		242	19		242	18
802.11ax_20MHz SISO_OFDMA	HE4	26	18	HE9	26	18
		52	18		52	18
		106	18		106	18
		242	18		242	18
	HE5	26	18	HE10	26	17.5
		52	18		52	17.5
		106	18		106	17.5
		242	18		242	17.5
				HE11	26	17.5
					52	17.5
					106	17.5
					242	17.5

Note: The specifications of RF output power are subject to change to fulfill the safety regulation and requirements in end-user product.

Sensitivity, tolerance ± 2 dB

CCK modulation PER ≦ 8%、OFDM modulation PER ≦ 10%

802.11b	Data Rate	Spec.(dBm)		
	1Mbps	-96		
	2Mbps	-90		
	5.5Mbps	-88		
	11Mbps	-87		
802.11g	Data Rate	Spec.(dBm)	Data Rate	Spec.(dBm)
	6Mbps	-91	24Mbps	-83
	9Mbps	-88	36Mbps	-80
	12Mbps	-87	48Mbps	-76
	18Mbps	-85	54Mbps	-73
802.11n_20MHz	Data Rate	Spec.(dBm)	Data Rate	Spec.(dBm)
	MCS0	-90	MCS4	-77
	MCS1	-85	MCS5	-75
	MCS2	-84	MCS6	-72
	MCS3	-80	MCS7	-71
802.11ax_20MHz	Data Rate	Spec.(dBm)	Data Rate	Spec.(dBm)
	HE0	-90	HE6	-72
	HE1	-85	HE7	-71

	HE2	-84	**HE8**	-69
	HE3	-80	**HE9**	-68
	HE4	-77	**HE10**	-67
	HE5	-75	**HE11**	-66
Maximum Input Level	802.11b : -10 dBm			
	802.11g/n/ax : -20 dBm			

3.2 5 RF Specification

Conditions : VBAT=3.3V ; VDDIO=1.8V ; Temp=25°C

Feature	Description
WLAN Standard	IEEE 802.11a/n/ac/ax & Wi-Fi compliant
Frequency Range	5150~5350MHz、5470~5725MHz、5725~5850MHz (5GHz UNII Band)
Number of Channels	5150~5350MHz：Ch36 ~ Ch64 5470~5725MHz：Ch100 ~ Ch140 5725~5850MHz：Ch149 ~ Ch165
Modulation	802.11a : OFDM /64-QAM、16-QAM、QPSK、BPSK 802.11n : OFDM /64-QAM、16-QAM、QPSK、BPSK 802.11ac : OFDM /256-QAM、64-QAM、16-QAM、QPSK、BPSK 802.11ax : OFDMA /1024-QAM、256-QAM、64-QAM、16-QAM、QPSK、BPSK

Output Power , tolerance ± 2 dB

The transmit EVM quality & spectrum mask are compliant with IEEE 802.11 standard

802.11a	**Frequency (MHz)**	**6~9Mbps**	**12~18Mbps**	**24Mbps**	**36Mbps**
	5150~5350	16	16	16	16
	5470~5725	16	16	16	16
	5725~5850	16	16	16	16
	Frequency (MHz)	**48Mbps**	**54Mbps**		
	5150~5350	16	16		
	5470~5725	16	16		
	5725~5850	16	16		
802.11n 20MHz	**Frequency (MHz)**	**MCS0~2**	**MCS3**	**MCS4**	**MCS5**
	5150~5350	16	16	16	16
	5470~5725	16	16	16	16
	5725~5850	16	16	16	16
	Frequency (MHz)	**MCS6**	**MCS7**		
	5150~5350	15	15		
	5470~5725	15	15		
	5725~5850	15	15		

802.11n 40MHz	Frequency (MHz)	MCS0~2	MCS3	MCS4	MCS5
	5150~5350	16	16	16	16
	5470~5725	16	16	16	16
	5725~5850	16	16	16	16
	Frequency (MHz)	MCS6	MCS7		
	5150~5350	15	15		
	5470~5725	15	15		
	5725~5850	15	15		
802.11ac 20MHz	Frequency (MHz)	MCS0~2	MCS3	MCS4	MCS5
	5150~5350	16	16	16	16
	5470~5725	16	16	16	16
	5725~5850	16	16	16	16
	Frequency (MHz)	MCS6	MCS7	MCS8	
	5150~5350	15	15	14	
	5470~5725	15	15	14	
	5725~5850	15	15	14	
802.11ac 40MHz	Frequency (MHz)	MCS0~2	MCS3	MCS4	MCS5
	5150~5350	16	16	16	16
	5470~5725	16	16	16	16
	5725~5850	16	16	16	16
	Frequency (MHz)	MCS6	MCS7	MCS8	MCS9
	5150~5350	15	15	14	14
	5470~5725	15	15	14	14
	5725~5850	15	15	14	14
802.11ac 80MHz	Frequency (MHz)	MCS0~2	MCS3	MCS4	MCS5
	5150~5350	16	16	16	16
	5470~5725	16	16	16	16
	5725~5850	16	16	16	16
	Frequency (MHz)	MCS6	MCS7	MCS8	MCS9
	5150~5350	15	14.5	14	13.5
	5470~5725	15	14.5	14	13.5
	5725~5850	15	14.5	14	13.5

802.11ax 20MHz	Frequency (MHz)	HE0~2	HE3	HE4	HE5
	5150~5350	16	16	16	16
	5470~5725	16	16	16	16
	5725~5850	16	16	16	16
	Frequency (MHz)	HE6	HE7	HE8	HE9
	5150~5350	15	15	14	14
	5470~5725	15	15	14	14
	5725~5850	15	15	14	14
	Frequency (MHz)	HE10	HE11		
	5150~5350	13.5	13		
	5470~5725	13.5	10		
	5725~5850	13.5	10		
802.11ax 40MHz	Frequency (MHz)	HE0~2	HE3	HE4	HE5
	5150~5350	16	16	16	16
	5470~5725	16	16	16	16
	5725~5850	16	16	16	16
	Frequency (MHz)	HE6	HE7	HE8	HE9
	5150~5350	15	15	14	14
	5470~5725	15	15	14	14
	5725~5850	15	15	14	14
	Frequency (MHz)	HE10	HE11		
	5150~5350	13	12.5		
	5470~5725	13	10		
	5725~5850	13	10		

802.11ax 80MHz	Frequency (MHz)	HE0~2	HE3	HE4	HE5
	5150~5350	16	16	16	16
	5470~5725	16	16	16	16
	5725~5850	16	16	16	16
	Frequency (MHz)	HE6	HE7	HE8	HE9
	5150~5350	15	14.5	14	13.5
	5470~5725	15	14.5	14	13.5
	5725~5850	15	14.5	14	13.5
	Frequency (MHz)	HE10	HE11		
	5150~5350	12.5	12		
	5470~5725	12.5	10		
	5725~5850	12.5	10		
Note: The specifications of RF output power are subject to change to fulfill the safety regulation and requirements in end-user product.					

	Dara rate	Tones	Frequency	Spec.(dBm)
802.11ax_20MHz	HE0~2	26	5150~5350	16
			5470~5725	16
			5725~5850	16
		52	5150~5350	16
			5470~5725	16
			5725~5850	16
		106	5150~5350	16
			5470~5725	16
			5725~5850	16
		242	5150~5350	16
			5470~5725	16
			5725~5850	16
	HE3~4	26	5150~5350	16
			5470~5725	16
			5725~5850	16
		52	5150~5350	16
			5470~5725	16
			5725~5850	16
		106	5150~5350	16
			5470~5725	16
			5725~5850	16
		242	5150~5350	16
			5470~5725	16
			5725~5850	16
	HE5~7	26	5150~5350	15
			5470~5725	15
			5725~5850	15
		52	5150~5350	15
			5470~5725	15
			5725~5850	15
		106	5150~5350	15
			5470~5725	15
			5725~5850	15
		242	5150~5350	15
			5470~5725	15
			5725~5850	15

	HE8~9	26	5150~5350	14
			5470~5725	14
			5725~5850	14
		52	5150~5350	14
			5470~5725	14
			5725~5850	14
		106	5150~5350	14
			5470~5725	14
			5725~5850	14
		242	5150~5350	14
			5470~5725	14
			5725~5850	14
	HE10~11	242	5150~5350	13
			5470~5725	10
			5725~5850	10

	Dara rate	Tones	Frequency	Spec.(dBm)
802.11ax_40MHz	HE0~2	26	5150~5350	16
			5470~5725	16
			5725~5850	16
		52	5150~5350	16
			5470~5725	16
			5725~5850	16
		106	5150~5350	16
			5470~5725	16
			5725~5850	16
		242	5150~5350	16
			5470~5725	16
			5725~5850	16
		484	5150~5350	16
			5470~5725	16
			5725~5850	16
	HE3~4	26	5150~5350	16
			5470~5725	16
			5725~5850	16
		52	5150~5350	16
			5470~5725	16
			5725~5850	16
		106	5150~5350	16
			5470~5725	16
			5725~5850	16
		242	5150~5350	16
			5470~5725	16
			5725~5850	16
		484	5150~5350	16
			5470~5725	16
			5725~5850	16
	HE5~7	26	5150~5350	15
			5470~5725	15
			5725~5850	15
		52	5150~5350	15
			5470~5725	15
			5725~5850	15

		106	5150~5350	15
			5470~5725	15
			5725~5850	15
		242	5150~5350	15
			5470~5725	15
			5725~5850	15
		484	5150~5350	15
			5470~5725	15
			5725~5850	15
	HE8~9	26	5150~5350	14
			5470~5725	14
			5725~5850	14
		52	5150~5350	14
			5470~5725	14
			5725~5850	14
		106	5150~5350	14
			5470~5725	14
			5725~5850	14
		242	5150~5350	14
			5470~5725	14
			5725~5850	14
		484	5150~5350	14
			5470~5725	14
			5725~5850	14
	HE10~11	242	5150~5350	12.5
			5470~5725	10
			5725~5850	10
		484	5150~5350	12.5
			5470~5725	10
			5725~5850	10

	Dara rate	Tones	Frequency	Spec.(dBm)
802.11ax_80MHz	HE0~2	26	5150~5350	16
			5470~5725	16
			5725~5850	16
		52	5150~5350	16
			5470~5725	16
			5725~5850	16
		106	5150~5350	16
			5470~5725	16
			5725~5850	16
		242	5150~5350	16
			5470~5725	16
			5725~5850	16
		484	5150~5350	16
			5470~5725	16
			5725~5850	16
		996	5150~5350	16
			5470~5725	16
			5725~5850	16
	HE3~4	26	5150~5350	16
			5470~5725	16
			5725~5850	16
		52	5150~5350	16
			5470~5725	16
			5725~5850	16
		106	5150~5350	16
			5470~5725	16
			5725~5850	16
		242	5150~5350	16
			5470~5725	16
			5725~5850	16
		484	5150~5350	16
			5470~5725	16
			5725~5850	16
		996	5150~5350	16
			5470~5725	16
			5725~5850	16

	HE5~7	26	5150~5350	14.5
			5470~5725	14.5
			5725~5850	14.5
		52	5150~5350	14.5
			5470~5725	14.5
			5725~5850	14.5
		106	5150~5350	14.5
			5470~5725	14.5
			5725~5850	14.5
		242	5150~5350	14.5
			5470~5725	14.5
			5725~5850	14.5
		484	5150~5350	14.5
			5470~5725	14.5
			5725~5850	14.5
		996	5150~5350	14.5
			5470~5725	14.5
			5725~5850	14.5
	HE8~9	26	5150~5350	13.5
			5470~5725	13.5
			5725~5850	13.5
		52	5150~5350	13.5
			5470~5725	13.5
			5725~5850	13.5
		106	5150~5350	13.5
			5470~5725	13.5
			5725~5850	13.5
		242	5150~5350	13.5
			5470~5725	13.5
			5725~5850	13.5
		484	5150~5350	13.5
			5470~5725	13.5
			5725~5850	13.5
		996	5150~5350	13.5
			5470~5725	13.5
			5725~5850	13.5
	HE10~11	242	5150~5350	12
			5470~5725	10

			5725~5850	10
		484	**5150~5350**	12
			5470~5725	10
			5725~5850	10
		996	**5150~5350**	12
			5470~5725	10
			5725~5850	10

Sensitivity, tolerance ± 1.5 dB CCK modulation PER ≦ 8%、OFDM modulation PER ≦ 10%				
802.11a	Data Rate	Spec.(dBm)	Data Rate	Spec.(dBm)
	6Mbps	-90	24Mbps	-83
	9Mbps	-90	36Mbps	-80
	12Mbps	-88	48Mbps	-75
	18Mbps	-86	54Mbps	-73
802.11n_20MHz	Data Rate	Spec.(dBm)	Data Rate	Spec.(dBm)
	MCS0	-90	MCS4	-79
	MCS1	-88	MCS5	-76
	MCS2	-86	MCS6	-73
	MCS3	-83	MCS7	-72
802.11n_40MHz	Data Rate	Spec.(dBm)	Data Rate	Spec.(dBm)
	MCS0	-88	MCS4	-77
	MCS1	-86	MCS5	-72
	MCS2	-83	MCS6	-70
	MCS3	-80	MCS7	-69
802.11ac_20MHz	Data Rate	Spec.(dBm)	Data Rate	Spec.(dBm)
	MCS0	-90	MCS5	-75
	MCS1	-88	MCS6	-73
	MCS2	-86	MCS7	-70
	MCS3	-83	MCS8	-68
	MCS4	-79		
802.11ac_40MHz	Data Rate	Spec.(dBm)	Data Rate	Spec.(dBm)
	MCS0	-88	MCS5	-72
	MCS1	-86	MCS6	-70
	MCS2	-83	MCS7	-69
	MCS3	-80	MCS8	-65
	MCS4	-76	MCS9	-64
802.11ac_80MHz	Data Rate	Spec.(dBm)	Data Rate	Spec.(dBm)
	MCS0	-85	MCS5	-68
	MCS1	-82	MCS6	-67
	MCS2	-79	MCS7	-65
	MCS3	-76	MCS8	-62
	MCS4	-73	MCS9	-61

802.11ax_20MHz	Data Rate	Spec.(dBm)	Data Rate	Spec.(dBm)
	HE0	-90	HE6	-73
	HE1	-88	HE7	-70
	HE2	-86	HE8	-68
	HE3	-83	HE9	-64
	HE4	-79	HE10	-59
	HE5	-75	HE11	-57
802.11ax_40MHz	Data Rate	Spec.(dBm)	Data Rate	Spec.(dBm)
	HE0	-88	HE6	-70
	HE1	-86	HE7	-69
	HE2	-83	HE8	-65
	HE3	-80	HE9	-64
	HE4	-76	HE10	-60
	HE5	-72	HE11	-55
802.11ax_80MHz	Data Rate	Spec.(dBm)	Data Rate	Spec.(dBm)
	HE0	-85	HE6	-67
	HE1	-82	HE7	-65
	HE2	-79	HE8	-62
	HE3	-76	HE9	-61
	HE4	-73	HE10	-57
	HE5	-68	HE11	-53
Maximum Input Level	802.11a/n/ac/ax : -30 dBm			

3.3 6GHz RF Specification

Conditions : VBAT=3.3V ; VDDIO=1.8V ; Temp=25°C

Feature	Description
WLAN Standard	IEEE 802.11ax & Wi-Fi compliant
Frequency Range	5925~7125MHz (6GHz U-NII5, U-NII6, U-NII-7, U-NII-8 Band)
Number of Channels	5925~6425MHz：6G1 ~ 6G93 6425~6525MHz：6G97 ~ 6G113 6525~6875MHz：6G117~6G181 6875~7125MHz：6G185~6G233
Modulation	802.11ax : OFDMA /1024-QAM、256-QAM、64-QAM、16-QAM、QPSK、BPSK

Output Power , tolerance ± 2 dB

The transmit EVM quality & spectrum mask are compliant with IEEE 802.11 standard

802.11ax 20MHz	Frequency (MHz)	HE0~2	HE3	HE4	HE5
	5925~6425	16	16	16	16
	6425~6525	16	16	16	16
	6525~6875	16	16	16	16
	6875~7125	16	16	16	16
	Frequency (MHz)	HE6	HE7	HE8	HE9
	5925~6425	15	15	14	14
	6425~6525	15	15	14	14
	6525~6875	14.5	14.5	13.5	13.5
	6875~7125	14.5	14.5	13.5	13.5
	Frequency (MHz)	HE10	HE11		
	5925~6425	13.5	12.5		
	6425~6525	13.5	12.5		
	6525~6875	13	10		
	6875~7125	13	12.5		
802.11ax 40MHz	Frequency (MHz)	HE0~2	HE3	HE4	HE5
	5925~6425	16	16	16	16
	6425~6525	16	16	16	16
	6525~6875	16	16	16	16
	6875~7125	16	16	16	16
	Frequency (MHz)	HE6	HE7	HE8	HE9
	5925~6425	14.5	14.5	13.5	13.5
	6425~6525	14.5	14.5	13.5	13.5
	6525~6875	14.5	14.5	13.5	13.5

	6875~7125	14.5	14.5	13.5	13.5
	Frequency (MHz)	HE10	HE11		
	5925~6425	13	12		
	6425~6525	13	12		
	6525~6875	13	10		
	6875~7125	13	12		
802.11ax 80MHz	Frequency (MHz)	HE0~2	HE3	HE4	HE5
	5925~6425	16	16	16	16
	6425~6525	16	16	16	16
	6525~6875	16	16	16	16
	6875~7125	16	16	16	16
	Frequency (MHz)	HE6	HE7	HE8	HE9
	5925~6425	14.5	14.5	13.5	13.5
	6425~6525	14.5	14.5	13.5	13.5
	6525~6875	14.5	14.5	13.5	13.5
	6875~7125	14.5	13.5	13.5	13.5
	Frequency (MHz)	HE10	HE11		
	5925~6425	13	12		
	6425~6525	13	12		
	6525~6875	13	10		
	6875~7125	13	12		

Note: The specifications of RF output power are subject to change to fulfill the safety regulation and requirements in end-user product.

Sensitivity, tolerance ± 2 dB, OFDM modulation PER ≦ 10%

	Data Rate	Spec.(dBm)	Data Rate	Spec.(dBm)
802.11ax_20MHz SISO	HE0	-88	HE6	-71
	HE1	-86	HE7	-68
	HE2	-84	HE8	-66
	HE3	-83	HE9	-62
	HE4	-77	HE10	-57
	HE5	-73	HE11	-55
802.11ax_40MHz SISO	Data Rate	Spec.(dBm)	Data Rate	Spec.(dBm)
	HE0	-86	HE6	-68
	HE1	-84	HE7	-67
	HE2	-81	HE8	-63
	HE3	-78	HE9	-62
	HE4	-74	HE10	-68

	HE5	-70	**HE11**	-53
802.11ax_80MHz SISO	**Data Rate**	**Spec.(dBm)**	**Data Rate**	**Spec.(dBm)**
	HE0	-83	**HE6**	-65
	HE1	-80	**HE7**	-63
	HE2	-77	**HE8**	-60
	HE3	-74	**HE9**	-59
	HE4	-71	**HE10**	-55
	HE5	-66	**HE11**	-51
Maximum Input Level	802.11ax : -30dBm			

4. Bluetooth Specification

4.1 Bluetooth Specification

Conditions : VBAT=3.3V ; VDDIO=1.8V ; Temp=25°C

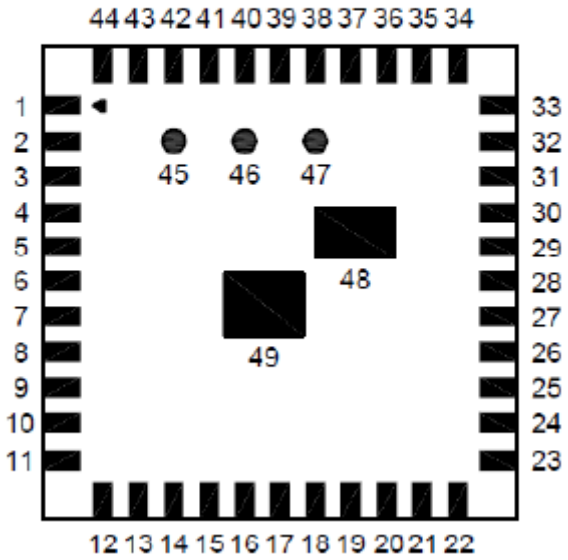
Feature	**Description**
General Specification	
Bluetooth Standard	BDR、EDR(1Mbps & 2Mbps)、LE(1Mbps)、2LE(2Mbps)
Host Interface	UART
Frequency Band	2402 MHz ~ 2480 MHz
Number of Channels	79 channels for classic、40 channels for BLE
Modulation	GFSK, π/4-DQPSK, 8DPSK
RF Specification	
Output Power , tolerance ± 1.5 dB	
	CL1 (dBm)
BDR Output Power	6
EDR Output Power	5
BLE Output Power	6
Sensitivity, tolerance ± 1.5 dB	
Sensitivity @ BER=0.1% for GFSK (1Mbps)	-87 dBm
Sensitivity @ BER=0.01% for π/4-DQPSK (2Mbps)	-87 dBm
Sensitivity @ BER=0.01% for 8DPSK (3Mbps)	-84 dBm
Sensitivity @ PER=30.8% for LE (1Mbps)	-90 dBm
Sensitivity @ PER=30.8% for 2LE (2Mbps)	-90 dBm
Maximum Input Level	GFSK (1Mbps):-20dBm
	π/4-DQPSK (2Mbps) :-20dBm
	8DPSK (3Mbps) :-20dBm

Note*：The Bluetooth BDR output power is able to be configured by firmware (hcd file).

5. Pin Definition

5.1 Pin Outline

<TOP VIEW>



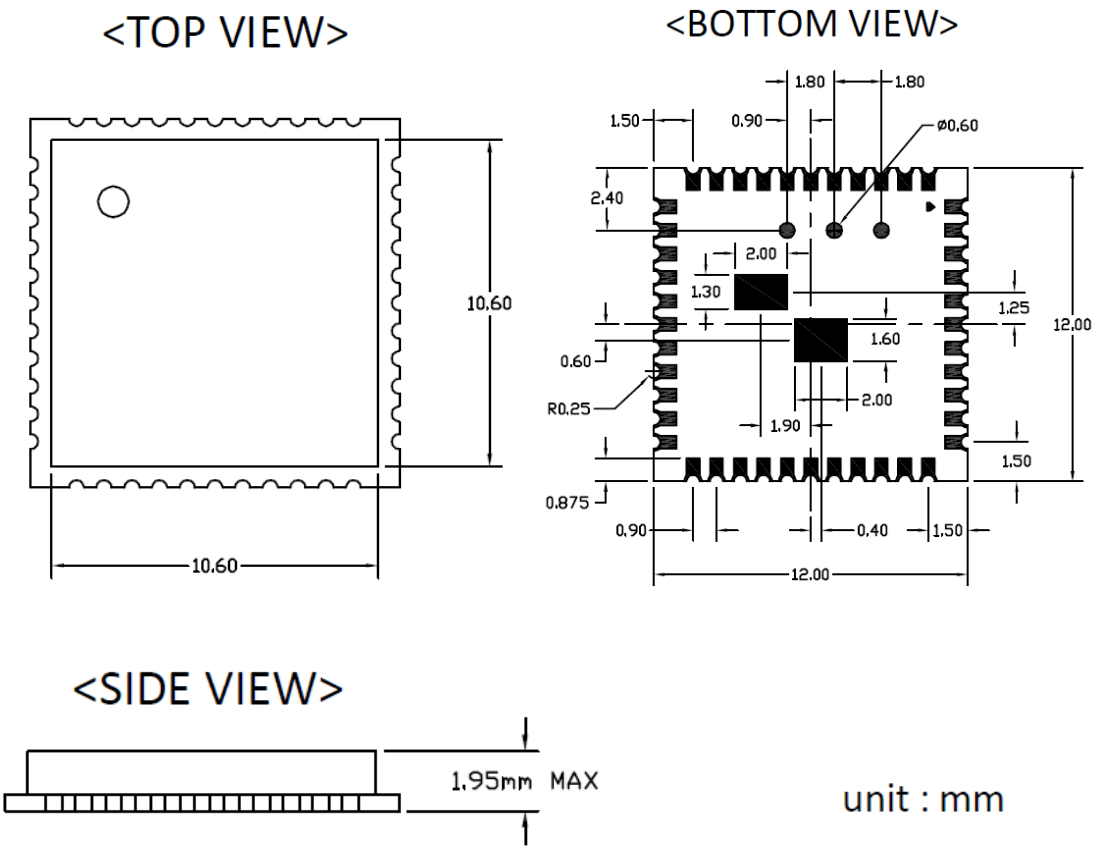
5.2 Pin Assignment

NO	Name	Type	Description
1	GND	—	Ground connections
2	NC	—	Floating.
3	GND	—	Ground connections
4	GND	—	Ground connections
5	WL_ANT0	I/O	RF I/O port0
6	GND	—	Ground connections
7	GND	—	Ground connections
8	PCM_OUT	O	PCM Data output
9	PCM_CLK	I/O	PCM clock
10	PCM_IN	I	PCM data input
11	PCM_SYNC	I/O	PCM sync signal
12	UART_CTS_N	I	Bluetooth UART interface
13	UART_RXD	I	Bluetooth UART interface
14	UART_TXD	O	Bluetooth UART interface
15	UART_RTS_N	O	Bluetooth UART interface
16	BT_DEV_WAKE	I	HOST wake-up Bluetooth device
17	BT_REG_ON	I	Low asserting reset for Bluetooth core
18	GND	—	Ground connections
19	WL_HOST_WAKE	O	WLAN to wake-up HOST and WL_GPIO_0
20	VBAT	P	Main power voltage source input
21	GND	—	Ground connections
22	CSR_VLX	O	Internal Buck voltage generation pin
23	CBUCK_0P72	I	Internal Buck voltage generation pin
24	GND	—	Ground connections
25	PCIE_TX_P	O	PCI Express transmit data-Positive
26	PCIE_TX_N	O	PCI Express transmit data-Negative
27	GND	—	Ground connections
28	PCIE_RX_P	I	PCI Express receive data-Positive
29	PCIE_RX_N	I	PCI Express receive data-Negative
30	GND	—	Ground connections
31	PCIE_RCLK_N	I	PCI Express differential clock input-Negative
32	PCIE_RCLK_P	I	PCI Express differential clock input-Positive
33	GND	—	Ground connections
34	LPO	I	External Low Power Clock input (32.768KHz)

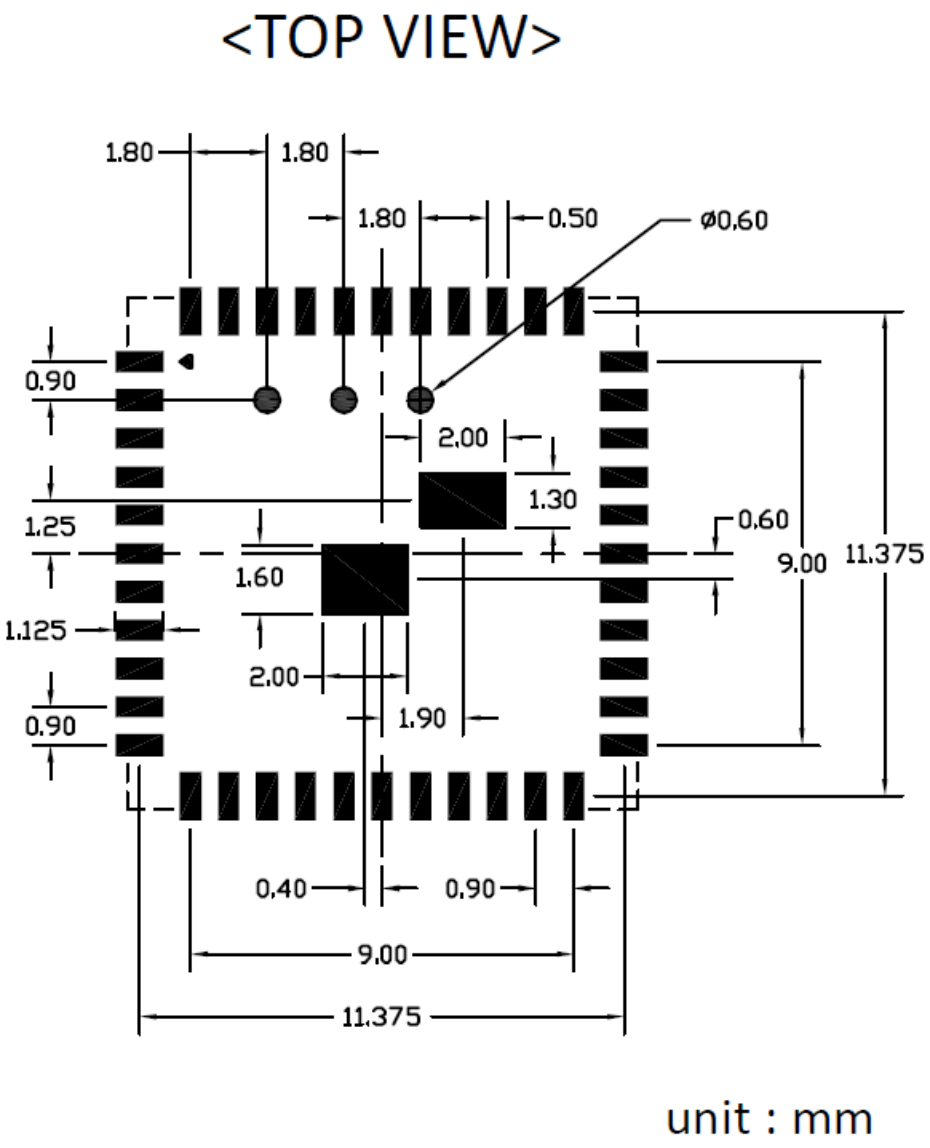
35	GND	—	Ground connections
36	XTAL_OUT	O	Crystal output
37	XTAL_IN	I	Crystal input
38	GND	—	Ground connections
39	BT_HOST_WAKE	O	Bluetooth device to wake-up HOST
40	PCIE_CLKREQ_L	OD	PCIe clock request
41	PCIE_PME_L	OD	PCI power management event output
42	PCIE_PREST_L	I	PCIe host indication to reset the device
43	VDDIO	P	I/O Voltage supply input
44	WL_REG_ON	I	Power up/down internal regulators used by WiFi section
45	GPIO_1	I/O	This pin can be programmed to be a GPIO, or the GCI external coexistence interface.
46	GPIO_2	I/O	This pin can be programmed to be a GPIO, or the GCI external coexistence interface.
47	GPIO_3	I/O	This pin can be programmed to be a GPIO, or the GCI external coexistence interface.
48	GND	—	Ground connections
49	GND	—	Ground connections

6. Dimensions

6.1 Module Dimensions



6.2 Recommended footprint



- Solder paste layer design is generally the same as recommended footprint.
  (錫膏層設計通常建議和焊墊尺寸相同)
- If soldering quality with good wetting on upright side is essential for PQC, how to optimize the aperture design in the stencil to adjust the amount of solder paste would be crucial.
  In addition, a kind of stencil design with stepped thickness in partial area would be considered if the thickness of stencil is about 0.1mm or thinner. Please optimize the stencil design by manufacture engineer or contact AMPAK FAE for assistance.
  (如果模組吃錫品質考量側面爬錫，如何優化鋼網開孔設計以調整適當的錫膏量是非常重要的。尤其鋼網的厚度大約是 0.1mm 或更薄時，可考慮局部加厚鋼網的設計。請諮詢製程工程師以優化鋼網的設計,或是聯絡正基科技技術支持團隊).

7. External clock reference

External LPO signal characteristics

Parameter	Specification	Units
Nominal input frequency	32.768	kHz
Frequency accuracy	+/-25	ppm
Duty cycle	30 - 70	%
Input signal amplitude	1.8±0.09	V
Signal type	Square-wave or sine-wave	-
Input impedance	>100k <5	Ω pF
Clock jitter (integrated over 300Hz – 15KHz)	<1	Hz
Output high voltage	0.7Vio - Vio	V

External 59.97MHz X'TAL characteristics

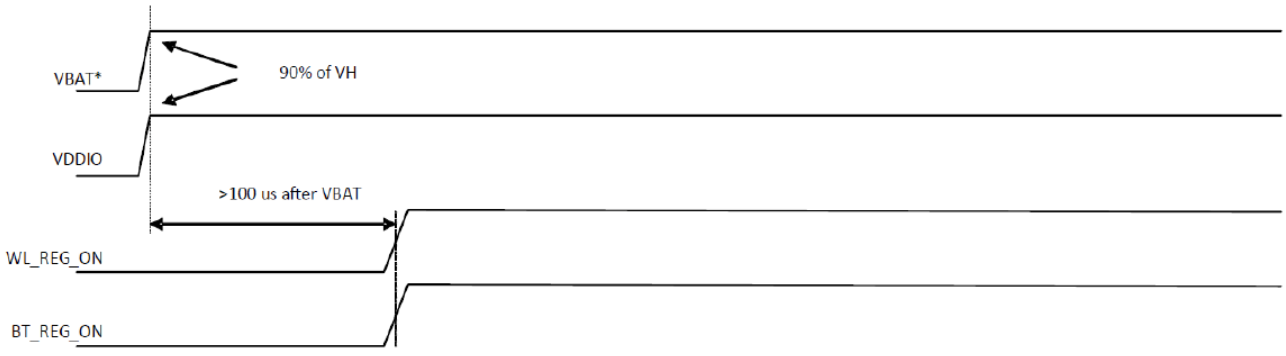
Parameter	Specification	Units
Nominal frequency - F0	59.97	MHz
Frequency Tolerance - ΔF / F 0 (At 25℃ +/- 3℃)	+/- 7	ppm
Operation Temperature Range - Topr	-30 ~ + 85	℃
Freq. Stability(over operating temperature) - TC Ref. to 25℃	+/- 10	ppm
Load capacitance - CL	8	pF
Equivalent Series Resistance – ESR	Max. 50	Ω
Drive Level - DL	Typ. 50, Max. 100	uW
Insulation resistance – IR At 100Vdc	Min. 500	MΩ

8. Host Interface Timing Diagram

8.1 Power-up Sequence Timing Diagram

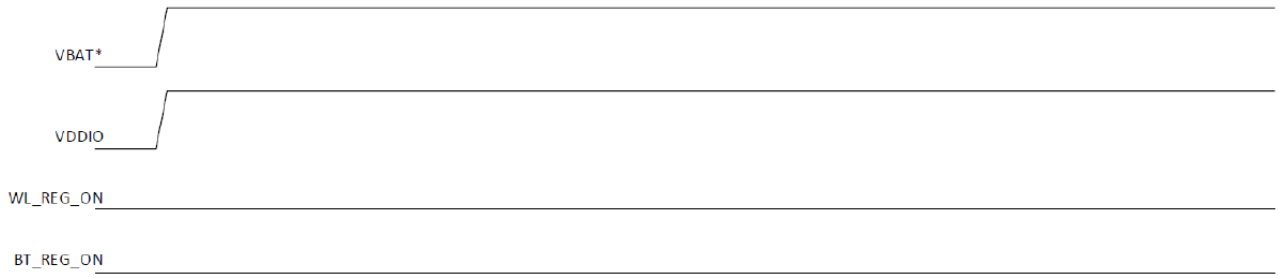
The module has signals that allow the host to control power consumption by enabling or disabling the Bluetooth, WLAN and internal regulator blocks. These signals are described below.
Additionally, diagrams are provided to indicate proper sequencing of the signals for carious operating states. The timing value indicated are minimum required values: longer delays are also acceptable.

- WL_REG_ON: Used by the PMU to power up or power down the internal regulators used by the WLAN section. When this pin is high, the regulators are enabled and the WLAN section is out of reset. When this pin is low the WLAN section is in reset.
- BT_REG_ON: Used by the PMU to power up or power down the internal regulators used by the BT section. Low asserting reset for Bluetooth. This pin has no effect on WLAN and does not control any PMU functions. This pin must be driven high or low (not left floating).



*Notes:
1. The VBAT and VDDIO 10%–90% rise-time slopes must be greater than 50 microseconds/V.
2. VBAT should be up before or at the same time as VDDIO. VDDIO should NOT be present first or be held high before VBAT is high.

WLAN=ON, Bluetooth=ON

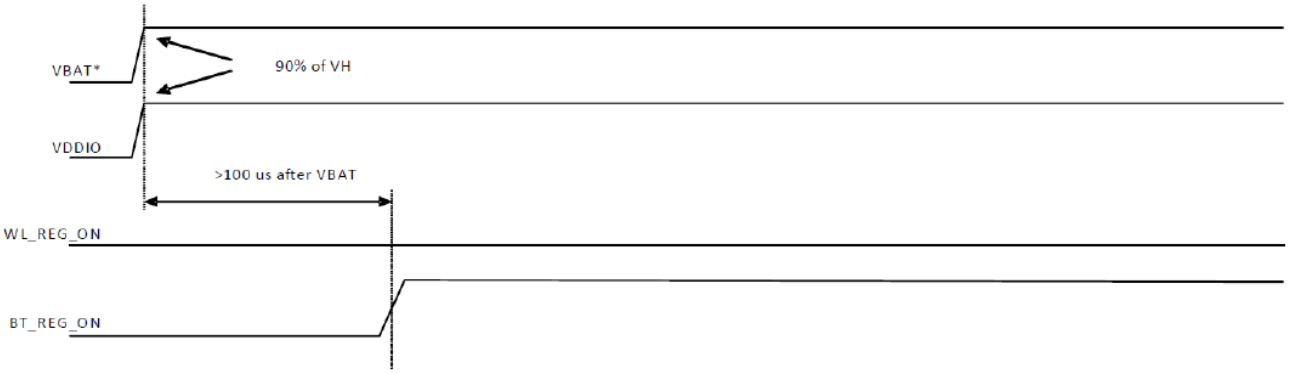


*Notes:
1. The VBAT and VDDIO 10%–90% rise-time slopes must be greater than 50 microseconds/V.
2. VBAT should be up before or at the same time as VDDIO. VDDIO should NOT be present first or be held high before VBAT is high.

WLAN=OFF, Bluetooth=OFF

***Notes:**
1. The VBAT and VDDIO 10%–90% rise-time slopes must be greater than 50 microseconds/V.
2. VBAT should be up before or at the same time as VDDIO. VDDIO should NOT be present first or be held high before VBAT is high.

WLAN=ON, Bluetooth=OFF



WLAN=OFF, Bluetooth=ON

8.2 PCIe Interface Description

The PCI Express(PCIe) core on the AP6781P is a high-performance serial I/O interconnect that is protocol compliant and electrically compatible with the PCI Express Base Specification v3.0 running at Gen1 speeds.

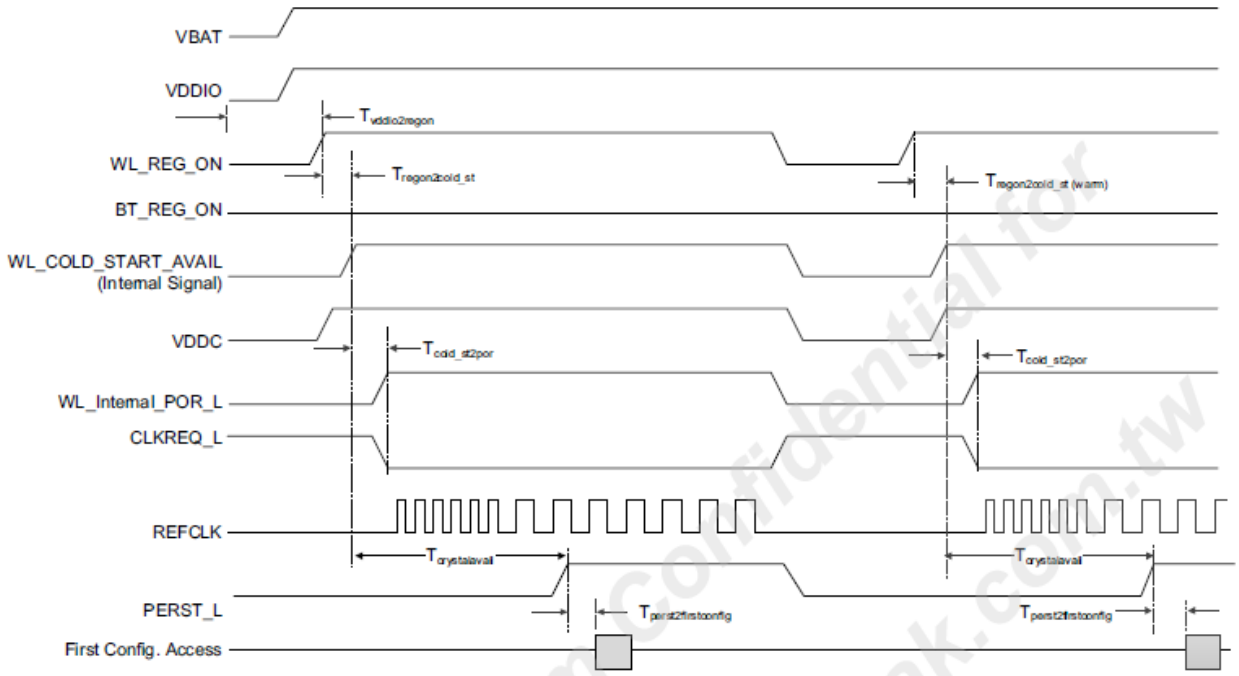
PCI Express Interface Parameters

Parameter	Symbol	Comments	Min.	Typ.	Max.	Unit
General[a]						
Baud rate	BPS	—	—	5	—	Gbaud
Reference clock peak-to-peak differential[b]	Vref	LVPECL, AC coupled	0.95	—	—	V
Receiver						
Differential termination	ZRX-DIFF-DC	Differential termination	80	100	120	Ω
DC impedance	ZRX-DC	DC common-mode impedance	40	50	60	Ω
Powered down termination (POS)	ZRX-HIGH-IMP-DC-POS	Power-down or RESET high impedance	100k	—	—	Ω
Powered down termination (NEG)	ZRX-HIGH-IMP-DC-NEG	Power-down or RESET high impedance	1k	—	—	Ω
Input voltage	VRX-DIFFp-p	AC coupled, differential p-p	175	—	—	mV
Jitter tolerance	TRX-EYE	Minimum receiver eye width	0.4	—	—	UI
Differential return loss	RLRX-DIFF	Differential return loss	10	—	—	dB
Common-mode return loss	RLRX-CM	Common-mode return loss	6	—	—	dB
Unexpected electrical idle enter detect threshold integration time	TRX-IDEL-DET-DIFF-ENTERTIME	An unexpected electrical idle must be recognized no longer than this time to signal an unexpected idle condition.	—	—	10	ms
Signal detect threshold	VRX-IDLE-DET-DIFFp-p	Electrical idle detect threshold	65	—	175	mV
Transmitter						
Output voltage	VTX-DIFFp-p	Differential p-p, programmable in 16 steps	0.8	—	1200	mV
Output voltage rise time	VTX-RISE	20% to 80%	0.125 (2.5 GT/s) 0.15 (5 GT/s)	—	—	UI
Output voltage fall time	VTX-FALL	80% to 20%	0.125 (2.5 GT/s) 0.15 (5 GT/s)	—	—	UI
RX detection voltage swing	VTX-RCV-DETECT	The amount of voltage change allowed during receiver detection.	—	—	600	mV

PCI Express Interface Parameters (Continued)

Parameter	Symbol	Comments	Min.	Typ.	Max.	Unit
TX AC peak common-mode voltage (5 GT/s)	VTX-CM-AC-PP	TX AC common mode voltage (5 GT/s)	—	—	100	mV
TX AC peak common-mode voltage (2.5 GT/s)	VTX-CM-AC-P	TX AC common mode voltage (2.5 GT/s)	—	—	20	mV
Absolute delta of DC common-mode voltage during L0 and electrical idle	VTX-CM-DC-ACTIVE-IDLE-DELTA	Absolute delta of DC common-mode voltage during L0 and electrical idle.	0	—	100	mV
Absolute delta of DC common-mode voltage between D+ and D-	VTX-CM-DC-LINE-DELTA	DC offset between D+ and D-	0	—	25	mV
Electrical idle differential peak output voltage	VTX-IDLE-DIFF-AC-p	Peak-to-peak voltage	0	—	20	mV
TX short circuit current	ITX-SHORT	Current limit when TX output is shorted to ground.	—	—	90	mA
DC differential TX termination	ZTX-DIFF-DC	Low impedance defined during signaling (parameter is captured for 5.0 GHz by RLTX-DIFF)	80	—	120	Ω
Differential return loss	RLTX-DIFF	Differential return loss	10 (min) for 0.05: 1.25 GHz	—	—	dB
Common-mode return loss	RLTX-CM	Common-mode return loss	6	—	—	dB
TX eye width	TTX-EYE	Minimum TX eye width	0.75	—	—	UI

PCIe Power-On Timing



Timing Parameter	Notes	Value[a]	Unit
$T_{vddio2regon}$	–	0.1	ms
$T_{regon2cold\_st}$	3.4 ms + 162 instruction-level parallelism (ILP) cycles	10.13	ms
T_{cold_st2por}	54 ILP cycles	2.24	ms
$T_{crystalavail}$	509 ILP cycles	21.17	ms
$T_{perst2firstconfig}$	–	6.0	ms
$T_{vddioon2firstconfig}$	$T_{vddio2regon} + T_{regon2cold\_st} + T_{crystalavail} + T_{perst2firstconfig}$	37.4[b]	ms
$T_{regon2cold\_st\ (warm)}$	162 ILP cycles	6.73	ms

a. The time values assume an ILP tolerance of ±30%.

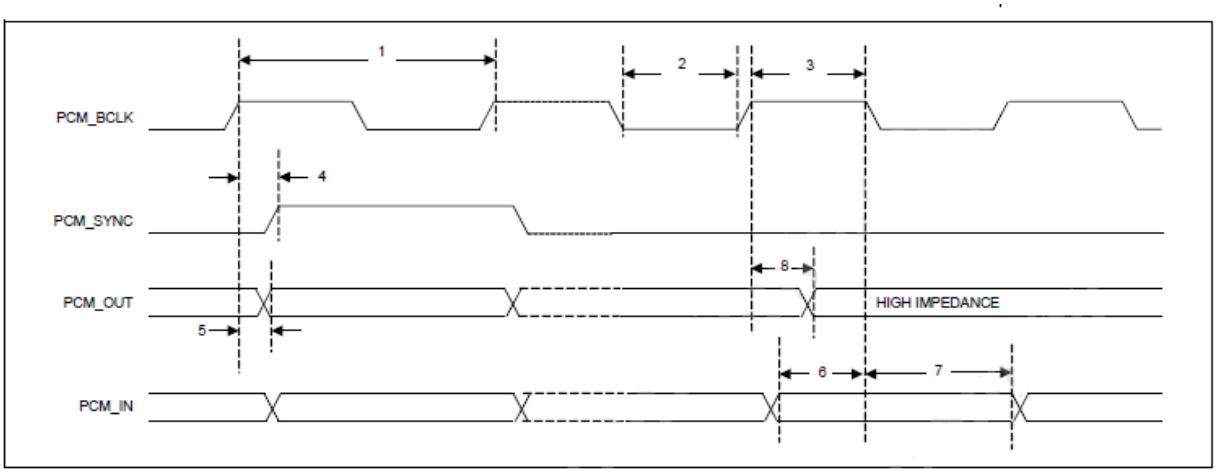
b. With VDDIO as a reference, 37.4 ms is the minimum system wait time before issuing the first configuration access.

8.3 PCM Interface Description

The PCM Interface on the AP6781P can connect to linear PCM Codec devices in master or slave mode. In master mode, the AP6781P generates the PCM_CLK and PCM_SYNC signals, and in slave mode, these signals are provided by another master on the PCM interface and are inputs to the AP6781P.The configuration of the PCM interface may be adjusted by the host through the use of vendor-specific HCI commands.

Short Frame Sync, Master Modem

PCM Timing Diagram (Short Frame Sync, Master Mode)

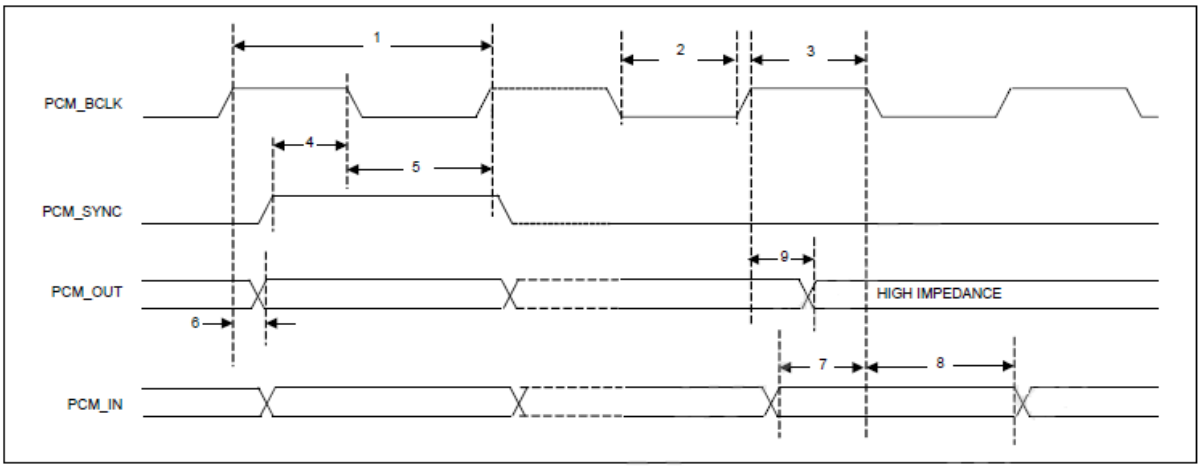


PCM Interface Timing Specifications (Short Frame Sync, Master Mode)

Reference	*Characteristics*	*Minimum*	*Typical*	*Maximum*	*Unit*
1	PCM bit clock frequency		–	12	MHz
2	PCM bit clock low	41	–	–	ns
3	PCM bit clock high	41	–	–	ns
4	PCM_SYNC delay	0	–	25	ns
5	PCM_OUT delay	0	–	25	ns
6	PCM_IN setup	8	–	–	ns
7	PCM_IN hold	8	–	–	ns
8	Delay from rising edge of PCM_BCLK during last bit period to PCM_OUT becoming high impedance	0	–	25	ns

Short Frame Sync, Slave Mode

PCM Timing Diagram (Short Frame Sync, Slave Mode)

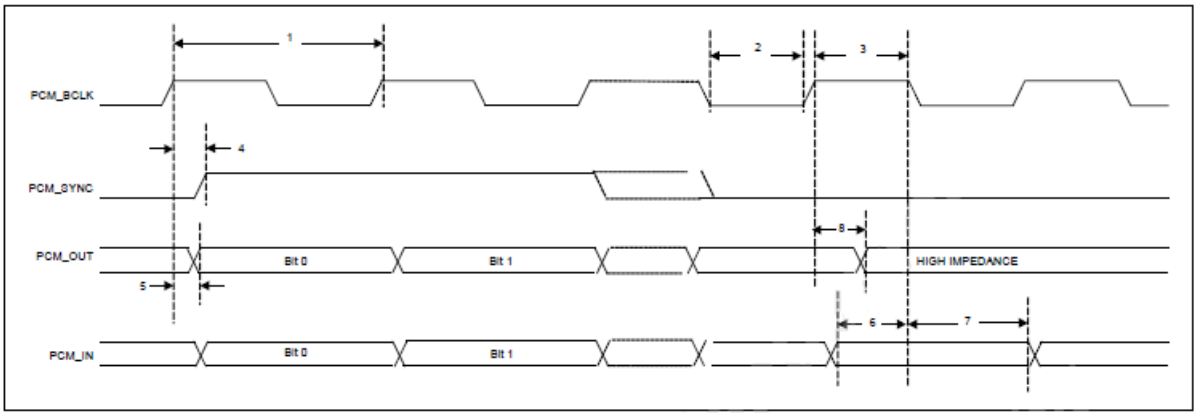


PCM Interface Timing Specifications (Short Frame Sync, Slave Mode)

Reference	Characteristics	Minimum	Typical	Maximum	Unit
1	PCM bit clock frequency	–	–	12	MHz
2	PCM bit clock low	41	–	–	ns
3	PCM bit clock high	41	–	–	ns
4	PCM_SYNC setup	8	–	–	ns
5	PCM_SYNC hold	8	–	–	ns
6	PCM_OUT delay	0	–	25	ns
7	PCM_IN setup	8	–	–	ns
8	PCM_IN hold	8	–	–	ns
9	Delay from rising edge of PCM_BCLK during last bit period to PCM_OUT becoming high impedance	0	–	25	ns

Long Frame Sync, Master Mode

PCM Timing Diagram (Long Frame Sync, Master Mode)

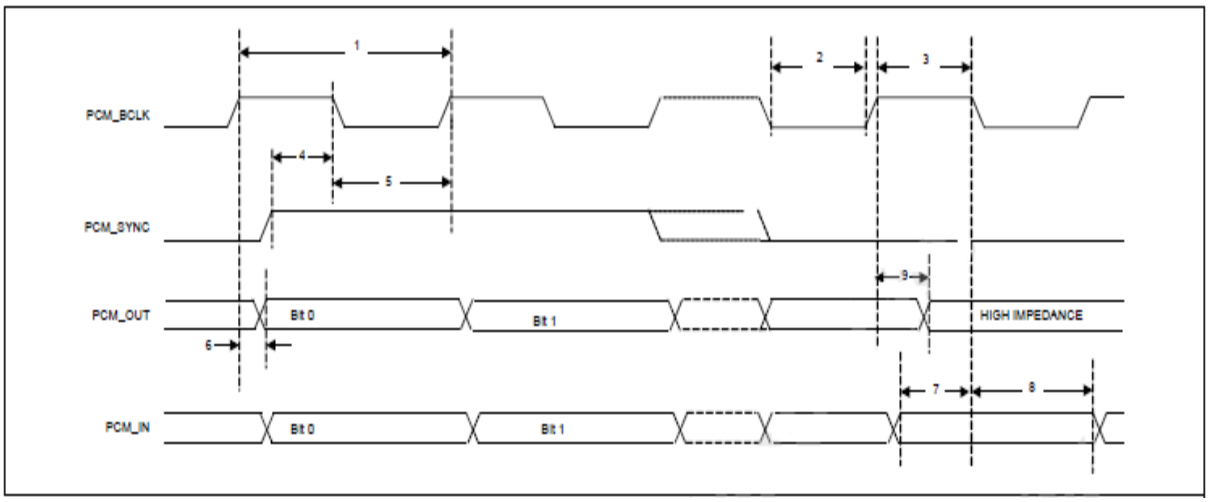


PCM Interface Timing Specifications (Long Frame Sync, Master Mode)

Reference	*Characteristics*	*Minimum*	*Typical*	*Maximum*	*Unit*
1	PCM bit clock frequency	–	–	12	MHz
2	PCM bit clock low	41	–	–	ns
3	PCM bit clock high	41	–	–	ns
4	PCM_SYNC delay	0	–	25	ns
5	PCM_OUT delay	0	–	25	ns
6	PCM_IN setup	8	–	–	ns
7	PCM_IN hold	8	–	–	ns
8	Delay from rising edge of PCM_BCLK during last bit period to PCM_OUT becoming high impedance	0	–	25	ns

Long Frame Sync, Slave Mode

PCM Timing Diagram (Long Frame Sync, Slave Mode)

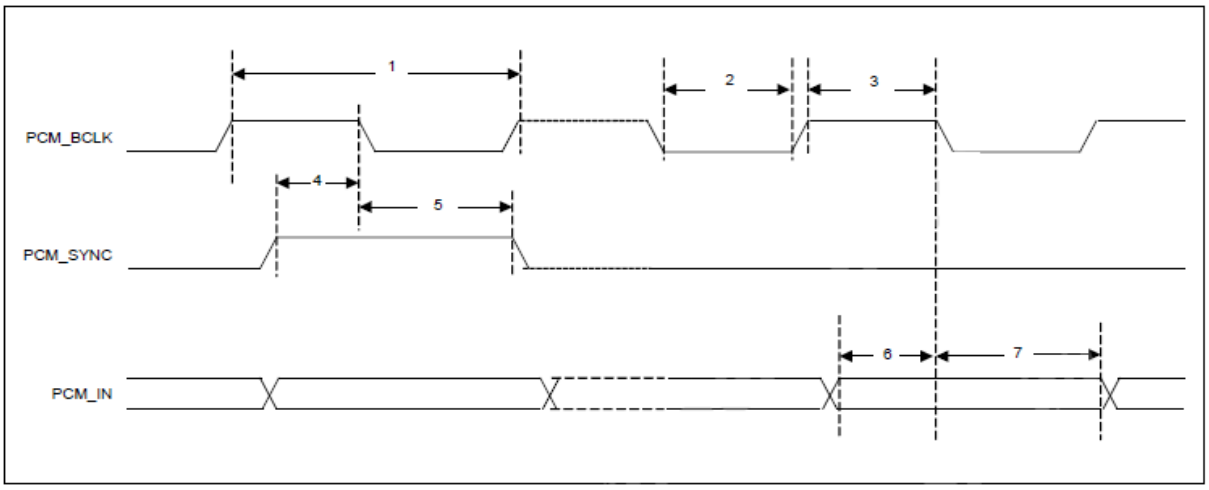


PCM Interface Timing Specifications (Long Frame Sync, Slave Mode)

Reference	*Characteristics*	*Minimum*	*Typical*	*Maximum*	*Unit*
1	PCM bit clock frequency	–	–	12	MHz
2	PCM bit clock low	41	–	–	ns
3	PCM bit clock high	41	–	–	ns
4	PCM_SYNC setup	8	–	–	ns
5	PCM_SYNC hold	8	–	–	ns
6	PCM_OUT delay	0	–	25	ns
7	PCM_IN setup	8	–	–	ns
8	PCM_IN hold	8	–	–	ns
9	Delay from rising edge of PCM_BCLK during last bit period to PCM_OUT becoming high impedance	0	–	25	ns

Short Frame Sync, Burst Mode

PCM Burst Mode Timing (Receive Only, Short Frame Sync)

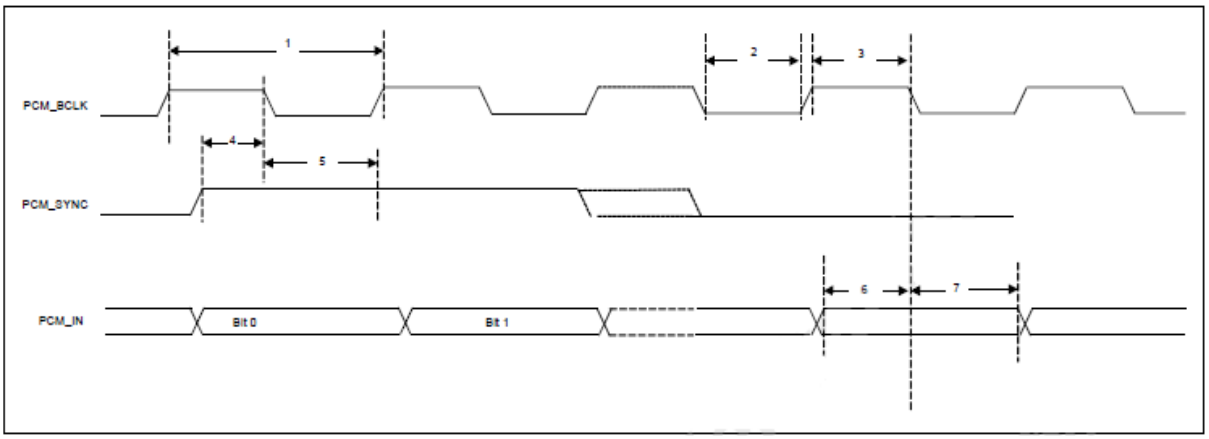


PCM Burst Mode (Receive Only, Short Frame Sync)

Reference	Characteristics	Minimum	Typical	Maximum	Unit
1	PCM bit clock frequency	–	–	24	MHz
2	PCM bit clock low	20.8	–	–	ns
3	PCM bit clock high	20.8	–	–	ns
4	PCM_SYNC setup	8	–	–	ns
5	PCM_SYNC hold	8	–	–	ns
6	PCM_IN setup	8	–	–	ns
7	PCM_IN hold	8	–	–	ns

Long Frame Sync, Burst Mode

PCM Burst Mode Timing (Receive Only, Long Frame Sync)



PCM Burst Mode (Receive Only, Long Frame Sync)

Reference	Characteristics	Minimum	Typical	Maximum	Unit
1	PCM bit clock frequency	–	–	24	MHz
2	PCM bit clock low	20.8	–	–	ns
3	PCM bit clock high	20.8	–	–	ns
4	PCM_SYNC setup	8	–	–	ns
5	PCM_SYNC hold	8	–	–	ns
6	PCM_IN setup	8	–	–	ns
7	PCM_IN hold	8	–	–	ns

8.4 UART Interface Description

The UART is a standard 4-wire interface (RX, TX, RTS, and CTS) with adjustable baud rates from 9600 bps to 4.0 Mbps. The interface features an automatic baud rate detection capability that returns a baud rate selection. Alternatively, the baud rate may be selected through a vendor-specific UART HCI command.

UART has a 1040-byte receive FIFO and a 1040-byte transmit FIFO to support EDR. Access to the FIFOs is conducted through the AHB interface through either DMA or the CPU. The UART supports the Bluetooth 5.0 UART HCI specification: H4, a custom Extended H4, and H5. The default baud rate is 115.2 Kbaud.

The UART supports the 3-wire H5 UART transport, as described in the Bluetooth specification (Three-wire UART Transport Layer). Compared to H4, the H5 UART transport reduces the number of signal lines required by eliminating the CTS and RTS signals.

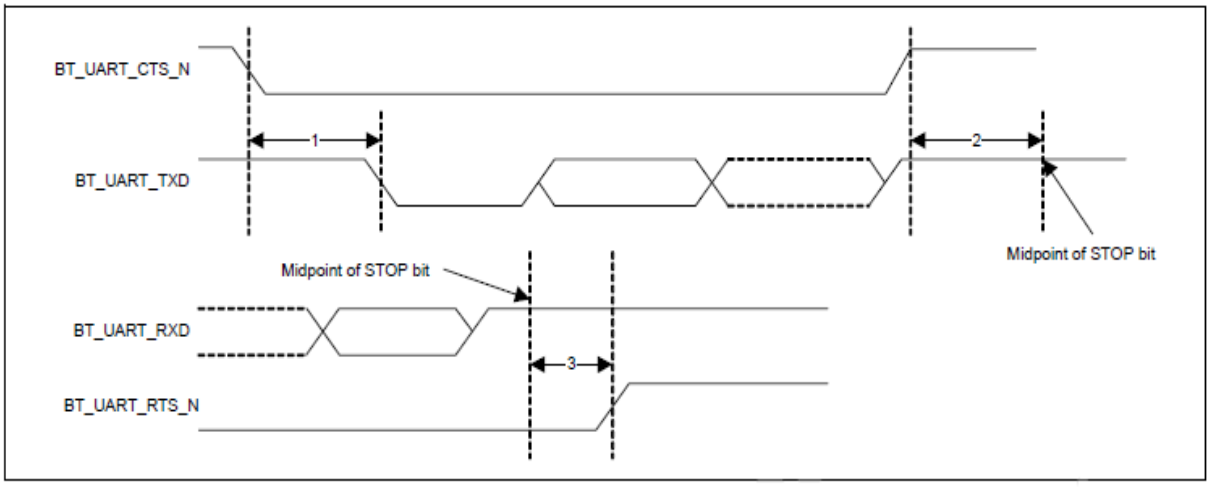
The UART can perform XON/XOFF flow control and includes hardware support for the Serial Line Input Protocol (SLIP). It can also perform wake-on activity. For example, activity on the RX or CTS inputs can wake the chip from a sleep state.

Normally, the UART baud rate is set by a configuration record downloaded after device reset, or by automatic baud rate detection, and the host does not need to adjust the baud rate. Support for changing the baud rate during normal HCI UART operation is included through a vendor-specific command that allows the host to adjust the contents of the baud rate registers. The UARTs operate correctly with the host UART as long as the combined baud rate error of the two devices is within ±2%.

Example of Common Baud Rates

Desired Rate	Actual Rate	Error (%)
4000000	4000000	0.00
3692000	3692308	0.01
3000000	3000000	0.00
2000000	2000000	0.00
1500000	1500000	0.00
1444444	1454544	0.70
921600	923077	0.16
460800	461538	0.16
230400	230796	0.17
115200	115385	0.16
57600	57692	0.16
38400	38400	0.00
28800	28846	0.16
19200	19200	0.00
14400	14423	0.16
9600	9600	0.00

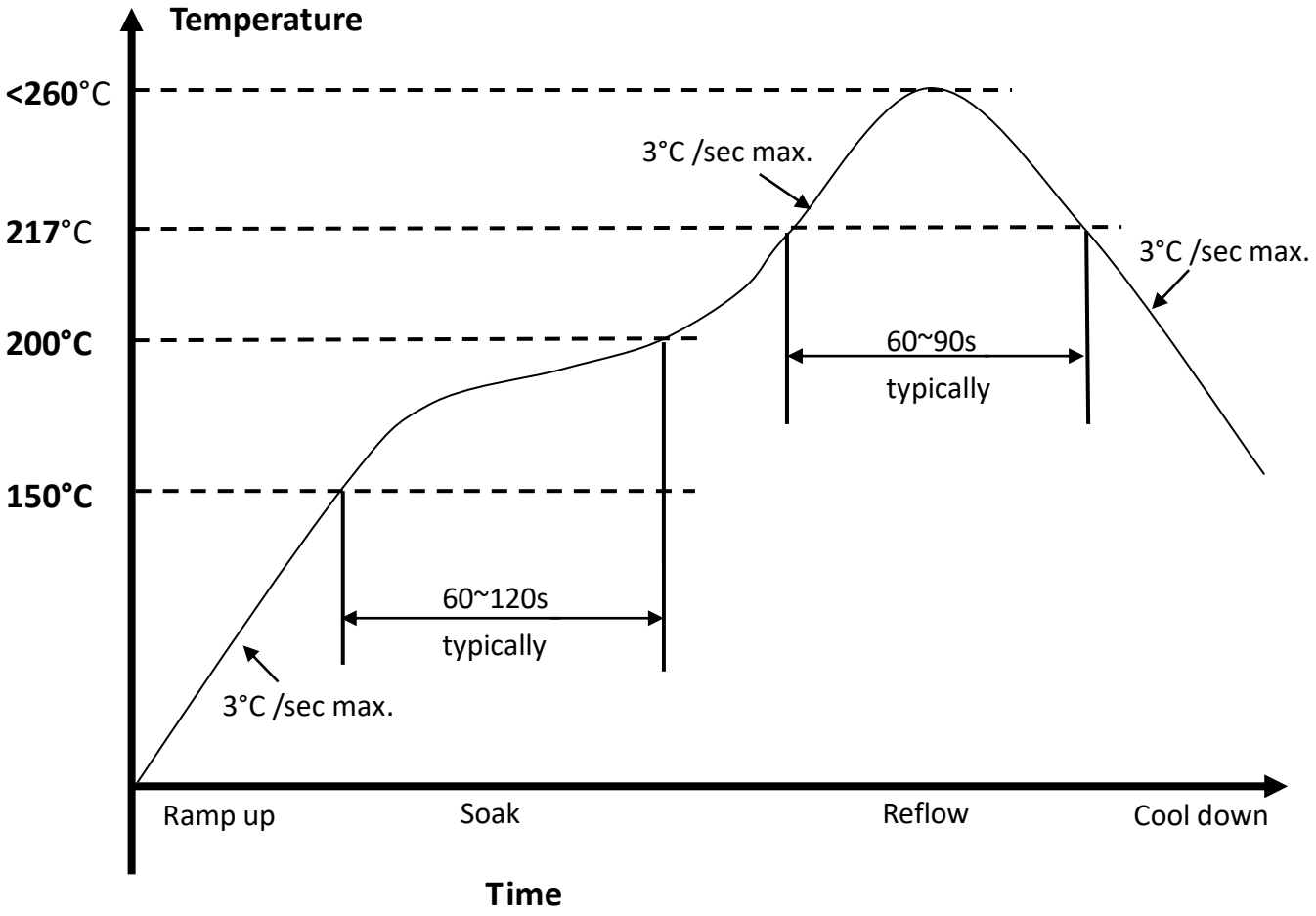
UART Timing



UART Timing Specifications

Ref	Characteristics	Min.	Typ.	Max.	Unit
1	Delay time, BT_UART_CTS_N low to BT_UART_TXD valid	–	–	1.5	Bit periods
2	Setup time, BT_UART_CTS_N high before midpoint of stop bit	–	–	0.5	Bit periods
3	Delay time, midpoint of stop bit to BT_UART_RTS_N high	–	–	0.5	Bit periods

9. Recommended Reflow Profile



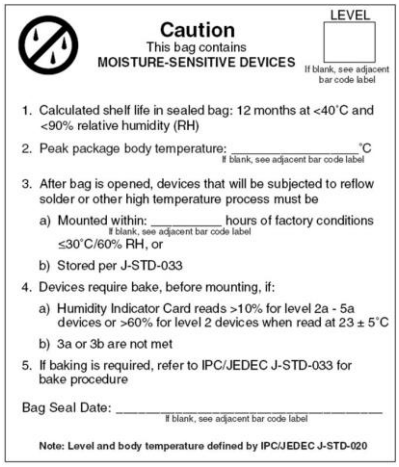
1. Referred to IPC/JEDEC standard
2. Peak Temperature : <260°C(Time within 5°C of actual Peak Temperature 20-40 seconds)
3. Cycle of Reflow : 2 times max.
4. Adding Nitrogen (N2) to implement 2000ppm or less of oxygen concentration during reflow process is recommended.
5. If the shelf time is exceeded, be sure baking step to remove the moisture from the component

10. Package Information

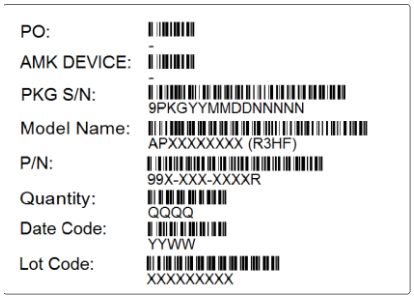
10.1 Label

Label A→ Anti-static and humidity notice

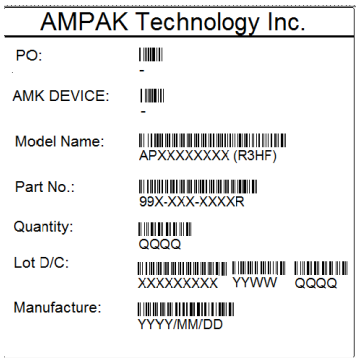
Label B→ MSL caution / Storage Condition



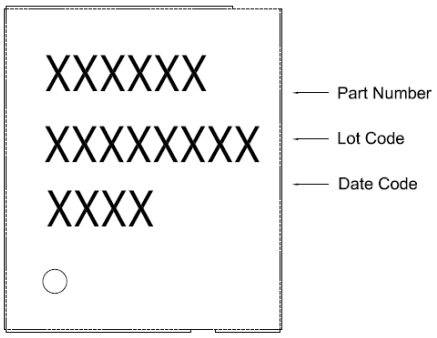
Label C→ Inner box label .

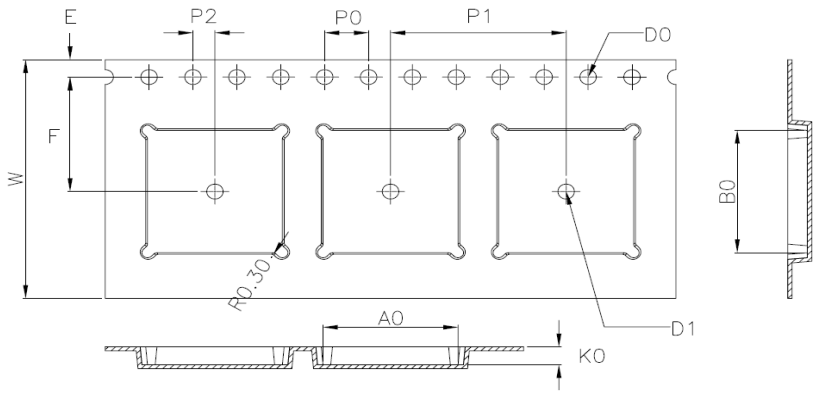


Label D→ Carton box label .



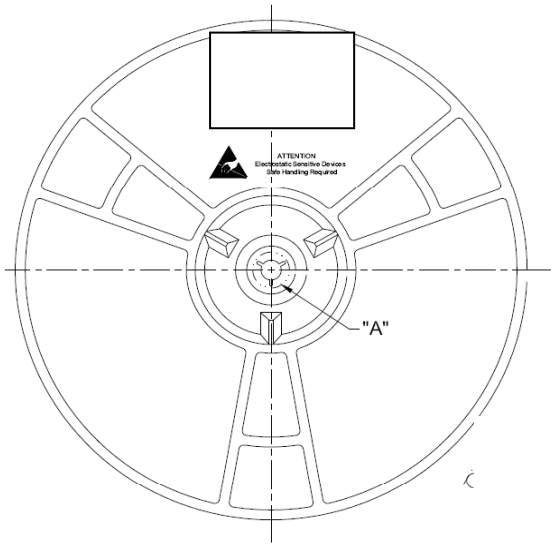
10.2 Dimension

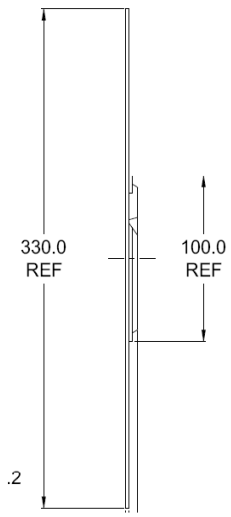


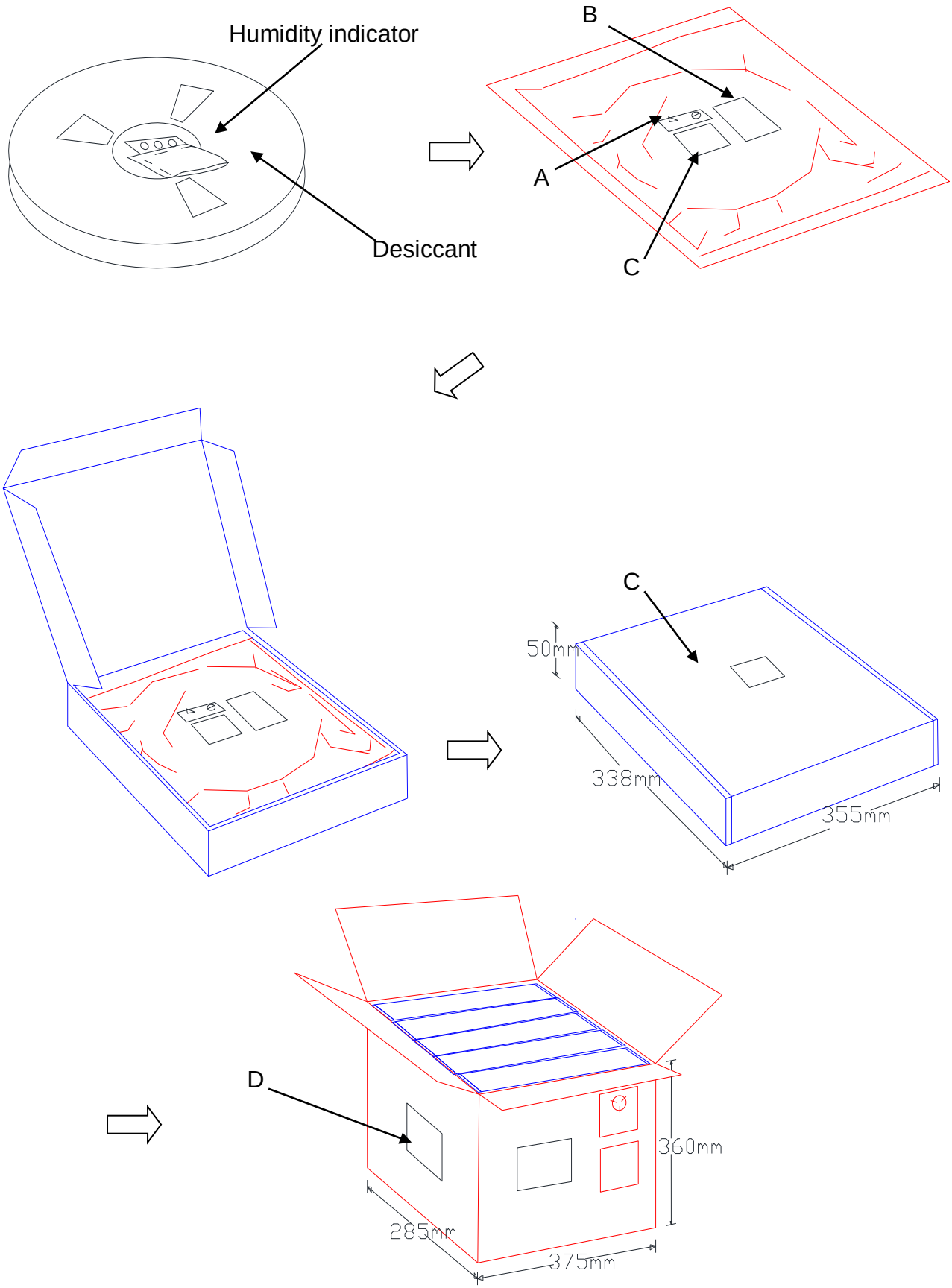


W	24.00±0.30
A0	12.30±0.10
B0	12.30±0.10
K0	1.80±0.10
E	1.75±0.10
F	11.50±0.10
P0	4.00±0.10
P1	16.00±0.10
P2	2.00±0.10
D0	1.50 +0.10 −0.00
D1	ø1.50MIN

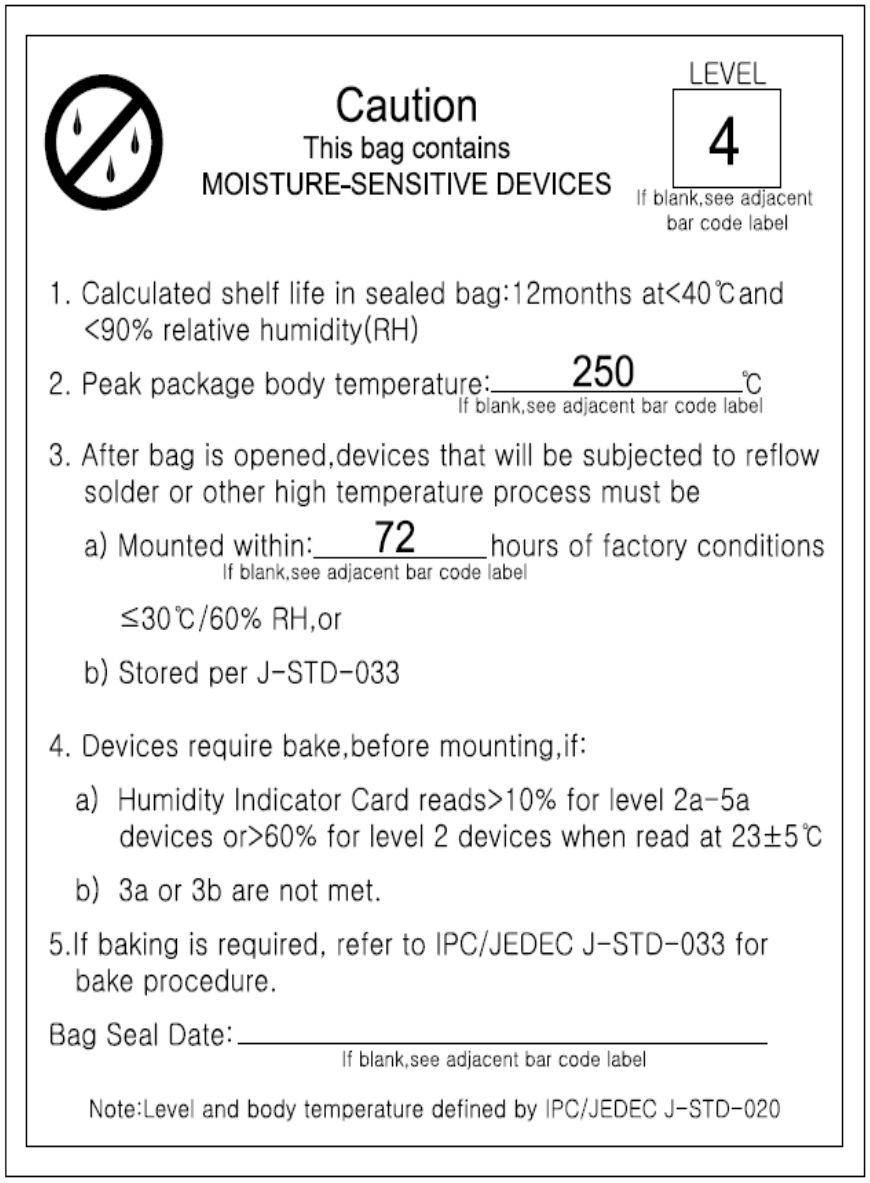
1. 10 sprocket hole pitch cumulative tolerance ±0.20.
2. Carrier camber is within 1 mm in 250 mm.
3. Material : Black Conductive Polystyrene Alloy.
4. All dimensions meet EIA-481-D requirements.
5. Thickness: 0.30±0.05mm.
6. Component load per 13”reel : 1000 pcs






Humidity indicator
Desiccant
B
A
C
C
50mm
338mm
355mm
D
360mm
285mm
375mm

10.3 MSL Level / Storage Condition



Caution
This bag contains
MOISTURE-SENSITIVE DEVICES

LEVEL 4
If blank,see adjacent bar code label

1. Calculated shelf life in sealed bag:12months at<40℃and <90% relative humidity(RH)
2. Peak package body temperature:250℃
   If blank,see adjacent bar code label
3. After bag is opened,devices that will be subjected to reflow solder or other high temperature process must be
   a) Mounted within:72 hours of factory conditions
      If blank,see adjacent bar code label
      ≤30℃/60% RH,or
   b) Stored per J-STD-033
4. Devices require bake,before mounting,if:
   a) Humidity Indicator Card reads>10% for level 2a-5a devices or>60% for level 2 devices when read at 23±5℃
   b) 3a or 3b are not met.
5. If baking is required, refer to IPC/JEDEC J-STD-033 for bake procedure.

Bag Seal Date:_____
If blank,see adjacent bar code label

Note:Level and body temperature defined by IPC/JEDEC J-STD-020